DELAY LOCKED LOOP FOR USE IN SYNCHRONOUS DYNAMIC RANDOM ACCESS MEMORY

ABSTRACT OF THE DISCLOSURE

A delay locked loop (DLL) for compensating for a skew in a synchronous dynamic random access memory includes: a delay model means for delaying an external clock signal by the skew to generate a delayed clock signal; a control unit, in response to the external clock signal and the delayed clock signal, for generating control signals, wherein the control signal includes a control clock signal, a delayed control signal, a replication signal and a replication enable signal; a first voltage controlled oscillator, in response to the control clock signal and the delayed control signal, for generating a measurement oscillating signal; a second voltage controlled oscillator, in response to the replication signal and the replication enable signal, for generating a replication oscillating signal; a first unit, in response to the measurement oscillating signal and the replication oscillating signal, for generating a DLL clock signal; and a second unit for comparing a phase difference between the DLL clock signal and the external clock signal to generate a voltage control signal, wherein time periods of the measurement oscillating signal and the replication oscillating signal are changed by the voltage control signal.